NEWS RELEASE

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LEADER IN POWER-EFFICIENT COMPUTER ARCHITECTURE RECEIVES ECKERT-MAUCHLY AWARD

Margaret Martonosi's Work Has Led to New Fields of Research

New York, NY, **June 7, 2021** – ACM, the Association for Computing Machinery, and the IEEE Computer Society have named Margaret Martonosi, the Hugh Trumbull Adams '35 Professor of Computer Science at Princeton University, as the recipient of the 2021 Eckert-Mauchly Award for contributions to the design, modeling, and verification of power-efficient computer architecture.

Martonosi has made significant contributions in computer architecture and microarchitecture, and her work has led to new fields of research. She has authored more than 175 publications (with 17,000 + citations) on subjects including parallel architectures, memory hierarchies, compilers, and mobile networks.

Power/Thermal Aware Architectures

Martonosi was an early innovator in the design and modeling of power-aware microarchitectures, including using narrow bit-widths, modeling and responding to thermal issues, and performing power estimation, e.g., as embodied in the ubiquitous Wattch tool.

In the area of narrow bit-widths, Martonosi co-authored (with David Brooks) the paper "Dynamically Exploiting Narrow Width Operands to Improve Processor Power and Performance." Martonosi and Brooks introduced two optimizations that greatly reduced processor power consumption. The paper earned the HPCA Test of Time Award, and the optimizations were licensed to Intel. Martonosi developed subsequent microarchitectural proposals that expanded on this work.

In a later (2001) paper with David Brooks "Dynamic Thermal Management for High-Performance Microprocessors," Martonosi investigated dynamic thermal management as a technique to control CPU power dissipation. Martonosi and Brooks demonstrated that, with appropriate thermal management, a CPU can be designed for a much lower maximum power rating, with minimal performance impact for typical applications. This was the first computer architecture paper to explicitly focus on thermal issues.

In a series of papers, Martonosi was also the first researcher to demonstrate how to use formal control-theoretic approaches to balance power and performance for dynamic voltage and frequency scaling (DVFS).

Power Simulation and Estimation

Martonosi recognized early the need for microarchitecture- and architecture-level power modeling and measurement infrastructure. She was a co-developer (with David Brooks and Vivek Tiwari) of Wattch, an architectural simulator that estimates CPU power consumption, which is used by thousands of researchers today. Wattch broke ground by demonstrating (against conventional wisdom) that accurate early-stage power models could be developed for early- stage microarchitectural design tradeoffs before more detailed computer-aided design (CAD) tools can be used. Martonosi also developed live runtime measurement tools for detailed power assessments of widely used and complex microprocessor systems.

ZebraNet Full-Stack Computing Platform

Martonosi broadened her scope beyond conventional computers to energy issues in mobile sensor networks, where energy fundamentally dictates system lifetime and data- gathering success.

Martonosi's ZebraNet Wildlife Tracking Project established the new research field of Mobile Sensor Networks. ZebraNet collected thousands of data points on Plains Zebras in Kenya. ZebraNet developed energy- efficient protocols for short- range, pairwise data transfers. Martonosi's work demonstrated that sparsely deployed mobile sensors could offer high data delivery rates and sensor coverage over large areas, at practical power budgets. ZebraNet provided biologists with never-before-seen animal behavior data. The work resulted in two test-of-time awards and several widely cited papers.

Memory Consistency Model Specification and Verification

Martonosi's ground-breaking work has demonstrated the potential of fast, early-stage, formal methods to verify the correctness of memory consistency model implementation. This work, embodied in the Check suite of verification tools, has had immediate and significant impact.

Modern hardware complexity also presents security challenges, and the Check suite includes efforts to provide rigorous and automated approaches for determining if a microarchitecture is susceptible to specified classes of security exploits. This kind of automatic checking will be fundamental to future information security.

Martonosi will be formally recognized with the ACM-IEEE CS Eckert-Mauchly Award during ACM/IEEE International Symposium on Computer Architecture (ISCA), which is being held virtually this year from June 14th-19th.

About the ACM-IEEE CS Eckert-Mauchly Award

ACM and IEEE Computer Society co-sponsor the Eckert-Mauchly Award, which was initiated in 1979. It recognizes contributions to computer and digital systems architecture and comes with a $5,000 prize. The award was named

for John Presper Eckert and John William Mauchly, who collaborated on the design and construction of the Electronic Numerical Integrator and Computer (ENIAC), the pioneering large-scale electronic computing machine, which was completed in 1947.

About ACM

ACM, the Association for Computing Machinery is the world's largest educational and scientific computing society, uniting computing educators, researchers and professionals to inspire dialogue, share resources and address the field's challenges. ACM strengthens the computing profession's collective voice through strong leadership, promotion of the highest standards, and recognition of technical excellence. ACM supports the professional growth of its members by providing opportunities for life-long learning, career development, and professional networking.

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